

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

TENTATIVE DATA
1,048,576 WORD × 1 BIT DYNAMIC RAM

DESCRIPTION

The TC511000AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 1bit organization
- Fast access time and cycle time

TC511000AP/AJ/AZ - 70/80/10			
t_{RAC} RAS Access Time	70ns	80ns	100ns
t_{AA} Column Address Access Time	35ns	40ns	50ns
t_{CAC} CAS Access Time	20ns	20ns	25ns
t_{AC} Cycle Time	130ns	150ns	180ns
t_{FC} Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator

Low Power

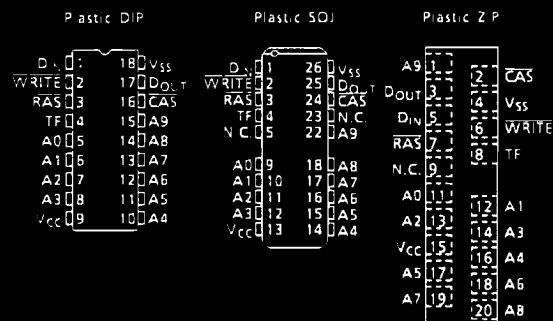
- 440mW MAX. Operating (TC511000AP/AJ/AZ - 70)
- 385mW MAX. Operating (TC511000AP/AJ/AZ - 80)
- 330mW MAX. Operating (TC511000AP/AJ/AZ - 10)
- 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package

TC511000AP	:	DIP18-P-300C
TC511000AJ	:	SOJ26-P-300
TC511000AZ	:	ZIP20-P-400

PIN NAMES

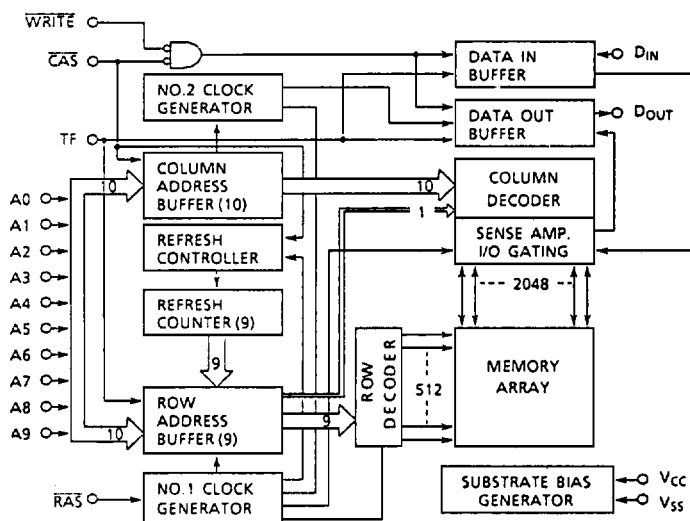
A0~A9 Address Inputs		WRITE !Read/Write Input	
RAS	Row Address Strobe	V_{CC}	Power (+ 5V)
D _{IN}	Data In	V_{SS}	Ground
D _{OUT}	Data Out	TF	Test Function
CAS	Column Address Strobe	N.C.	No Connection

PIN CONNECTION



TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	-1~7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1~10.5	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	$V_{CC} + 4.5$	-	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	-1.0	-	$V_{CC} + 1.0$	V	2

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I _{CC1}	OPERATING CURRENT	TC511000AP/AJ/AZ-70	—	80	mA	3, 4, 5
	Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511000AP/AJ/AZ-80	—	70		
		TC511000AP/AJ/AZ-10	—	60		
I _{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		—	2	mA	
I _{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT	TC511000AP/AJ/AZ-70	—	80	mA	3, 5
	Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ MIN.)	TC511000AP/AJ/AZ-80	—	70		
		TC511000AP/AJ/AZ-10	—	60		
I _{CC4}	FAST PAGE MODE CURRENT	TC511000AP/AJ/AZ-70	—	60	mA	3, 4, 5
	Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511000AP/AJ/AZ-80	—	50		
		TC511000AP/AJ/AZ-10	—	40		
I _{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		—	1	mA	
I _{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT	TC511000AP/AJ/AZ-70	—	80	mA	3
	Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511000AP/AJ/AZ-80	—	70		
		TC511000AP/AJ/AZ-10	—	60		
I _{I(L)}	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = $0V$)		— 10	10	μA	
I _{ITF(L)}	INPUT LEAKAGE CURRENT (only TF) ($0V \leq V_{IN(TF)} \leq V_{CC} + 0.5V$, All Other Pins Not Under Test = $0V$)		— 10	10	μA	
I _{O(L)}	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		— 10	10	μA	
I _{TF}	TEST FUNCTION INPUT CURRENT ($V_{CC} + 4.5V \leq V_{IN(TF)} \leq 10.5V$)		—	1	mA	
V _{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	—	V	
V _{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		—	0.4	V	

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)(Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC511000AP/ AJ/AZ-70		TC511000AP/ AJ/AZ-80		TC511000AP/ AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	—	150	—	180	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	—	175	—	210	—	ns	
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	55	—	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	65	—	70	—	85	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	—	25	ns	9,14
t_{AA}	Access Time from Column Address	—	35	—	40	—	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	50	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	60	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	25	—	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	—	40	—	50	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	—	60	—	75	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	50	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	11
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	CHARACTERISTIC	TC511000AP/ AJ/AZ-70		TC511000AP/ AJ/AZ-80		TC511000AP/ AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{WCR}	Write Command Hold Time referenced to $\overline{\text{RAS}}$	55	-	60	-	75	-	ns	
t _{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	20	-	20	-	25	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	20	-	20	-	25	-	ns	
t _{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t _{DH}	Data Hold Time	15	-	15	-	20	-	ns	12
t _{DHR}	Data Hold Time referenced to $\overline{\text{RAS}}$	55	-	60	-	75	-	ns	
t _{REF}	Refresh Period	-	8	-	8	-	8	ms	
t _{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time	20	-	20	-	25	-	ns	13
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay Time	70	-	80	-	100	-	ns	13
t _{AWD}	Column Address to $\overline{\text{WRITE}}$ Delay Time	35	-	40	-	50	-	ns	13
t _{CPWD}	$\overline{\text{CAS}}$ Precharge to $\overline{\text{WRITE}}$ Delay Time	35	-	40	-	50	-	ns	13
t _{CSR}	$\overline{\text{CAS}}$ Set-Up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	5	-	5	-	5	-	ns	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	15	-	15	-	20	-	ns	
t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	-	0	-	0	-	ns	
t _{CPT}	$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t _{TES}	Test Mode Enable Set-Up Time referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	
t _{TEHR}	Test Mode Enable Hold Time referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	
t _{TEHC}	Test Mode Enable Hold Time referenced to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	

CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1\text{MHz}$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C _{i1}	Input Capacitance (A0~A9, D _{IN})	-	5	pF
C _{i2}	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$, TF)	-	7	
C _o	Output Capacitance (D _{OUT})	-	7	

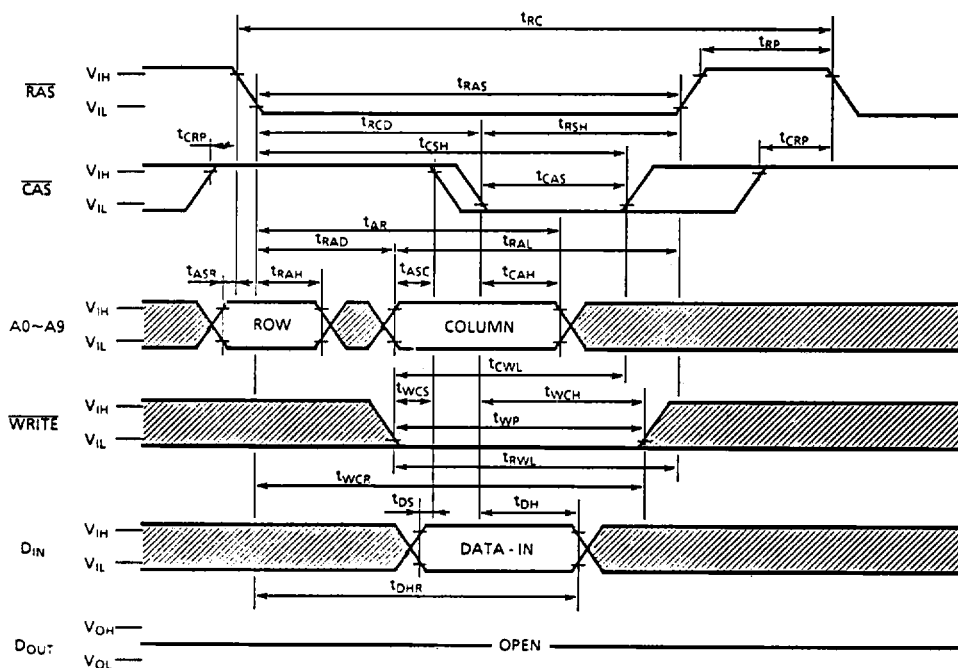
TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. $ICC1$, $ICC3$, $ICC4$, $ICC6$ depend on cycle rate.
4. $ICC1$, $ICC4$ depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5$ ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS} , t_{RWd} , t_{CWD} , t_{AWd} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWd} \geq t_{RWd}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWd} \geq t_{AWd}(\text{min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{min.})$ (Fast Page Mode), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
15. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RAD}(\text{max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

WRITE CYCLE (EARLY WRITE)

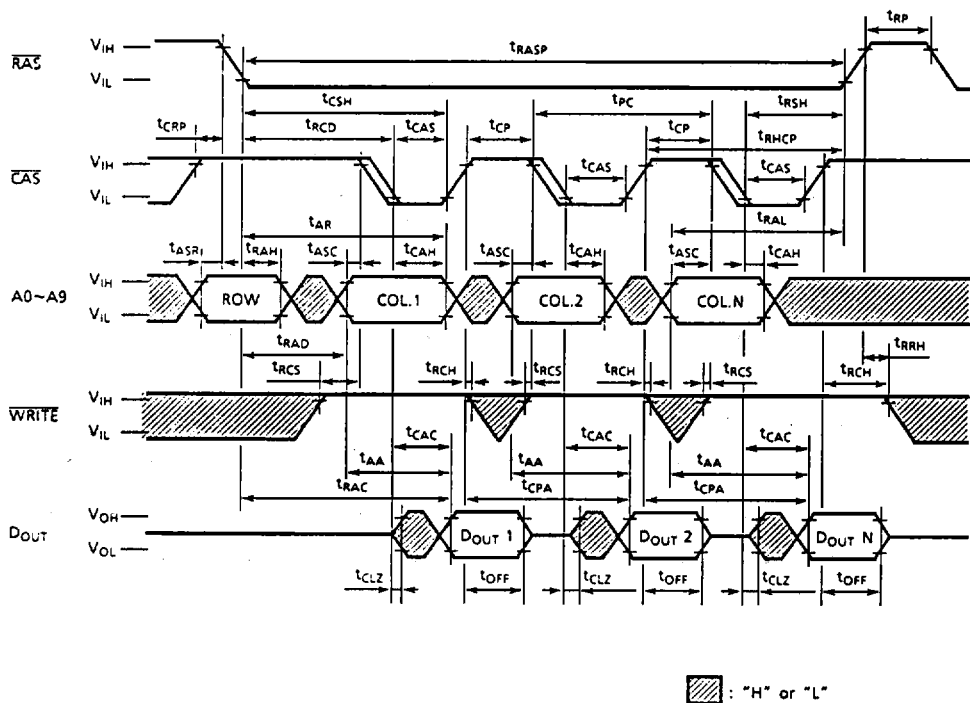


▨: "H" or "L"

NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

**TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80
TC511000AP/AJ/AZ-10**

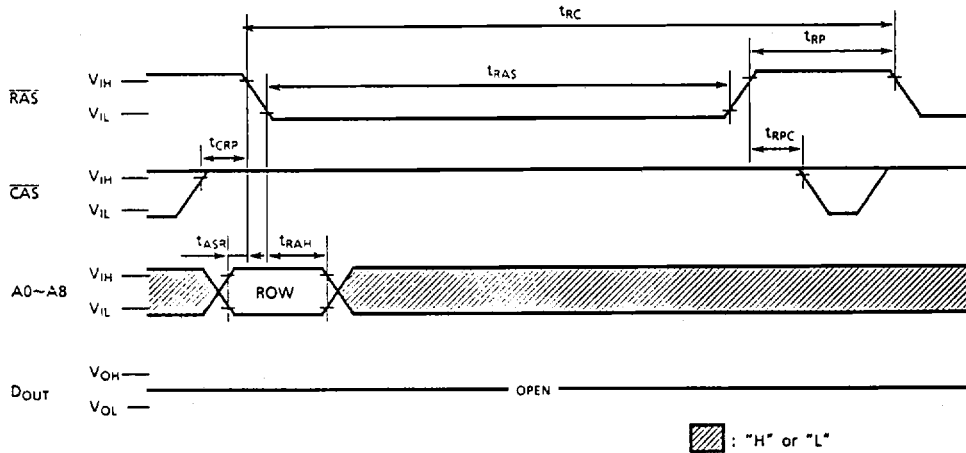
FAST PAGE MODE READ CYCLE



NOTE: "TF" pin should be connected to $V_{IL}(TF)$ level or open, if "Test Mode" is not used.

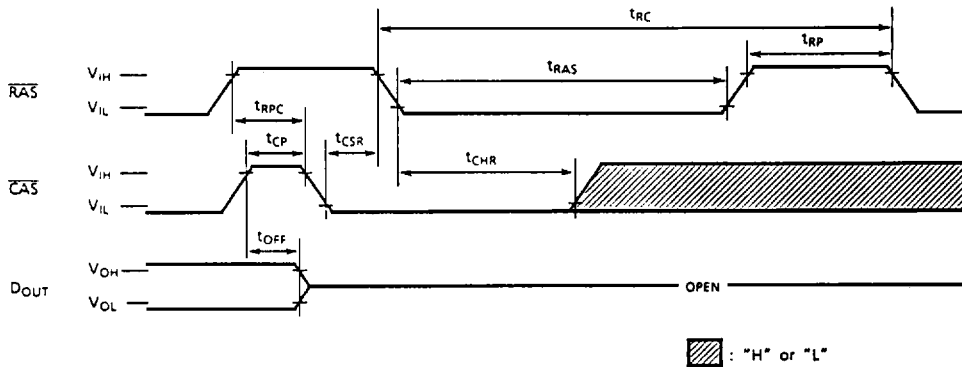
TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

RAS ONLY REFRESH CYCLE



NOTE: WRITE = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

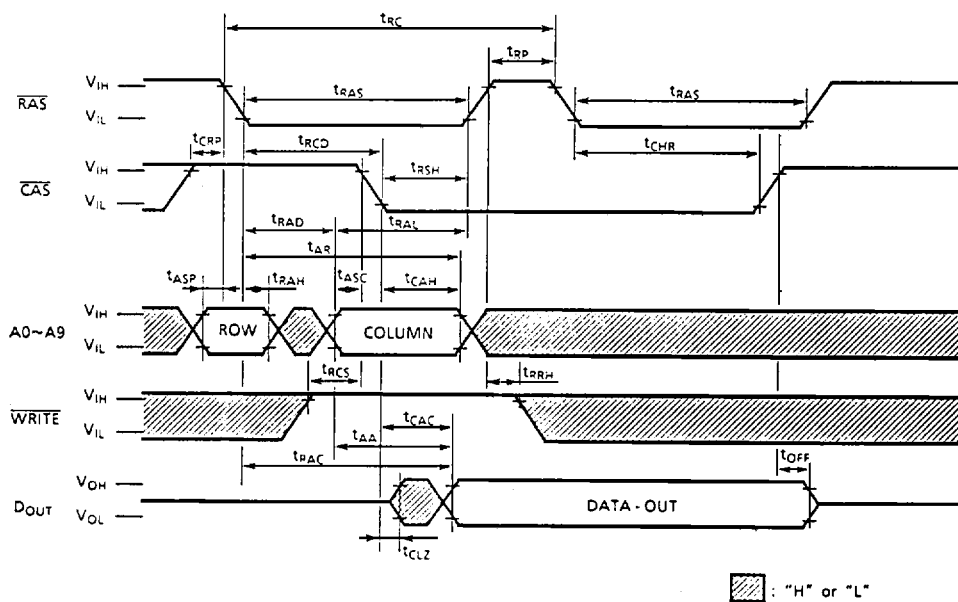
CAS BEFORE RAS REFRESH CYCLE



NOTE: WRITE = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

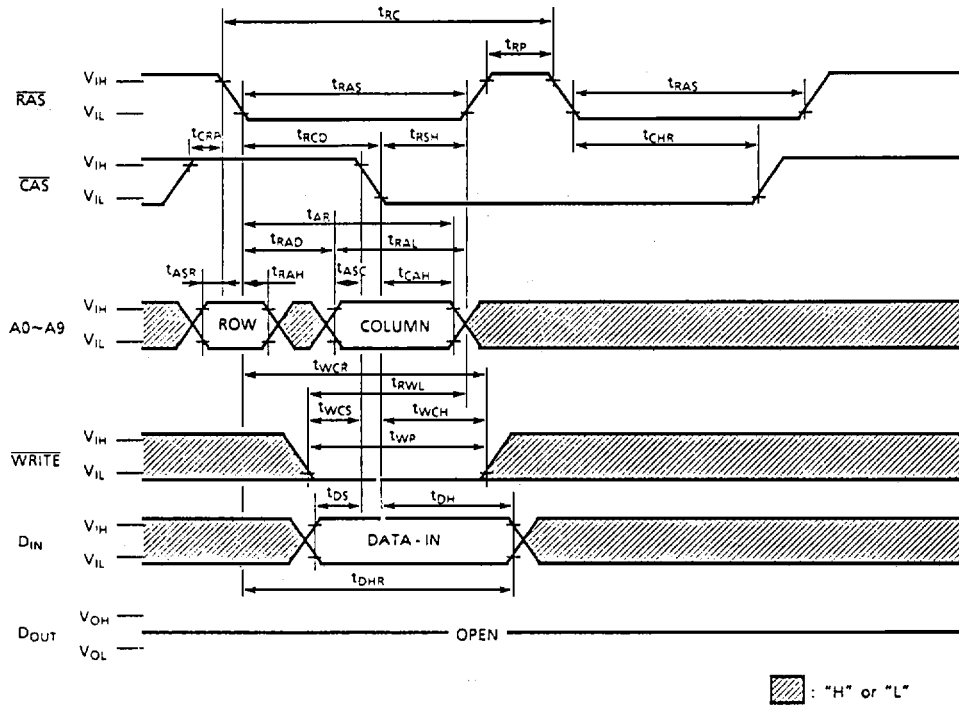
HIDDEN REFRESH CYCLE (READ)



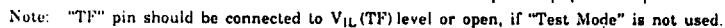
NOTE: "TF" pin should be connected to $V_{IL}(TF)$ level or open, if "Test Mode" is not used.

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.



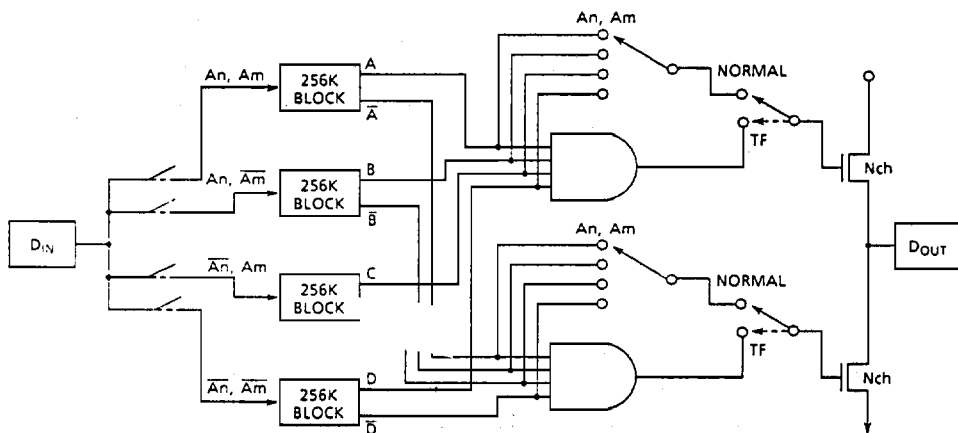
TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

TEST MODE

The TC511000AP/AJ/AZ is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511000AP/AJ/AZ including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

"Test Mode" function is performed on any of the timing cycles including Fast Page Mode when "TF" pin is held on "super voltage ($V_{CC} + 4.5V$ ($V_{CC} = 5V \pm 10\%$), max. voltage = $10.5V$)" for the specified period (t_{TES} , t_{TEHR} and t_{TEHC} ; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using 'N test pattern).

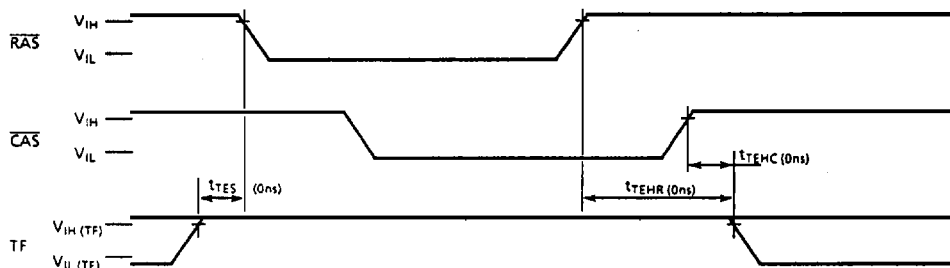


Fig. 2 Test Mode Cycle